Knowing your ARM from your ARSE

(or, how to identify the CPU features in your phone)

Embedded Recipes, Paris

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Disclaimer/excuses:

I no longer work at Arm!

Arm are sponsoring this conference and have kindly paid for my travel to be here.

I usually give fairly deep, low-level technical presentations, so this is a change for me.
Feel free to stop/interrupt me during the talk.

This presentation is based on work done at Arm and is not part of my current employment

Introduction

- Linux kernel co-maintainer of `arm64` architecture, `ARM` perf backends, `SMMU` drivers, atomics, locking, memory model, TLB invalidation…
- Worked for a decade in the Open-Source Software group at Arm
- Contributed significantly to the Armv8 architecture
- Heavy exposure to the development of the Arm ecosystem
- Tend to be CPU centric

Lots of insider knowledge required to overcome hurdles and develop successful system software for Arm…

Spot the difference

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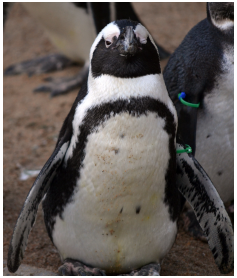
- Although the `Cortex-A32` also implements `Armv8` but is 32-bit only

Even Pinhead is confused (July, 2012)



*"They have separate versions for their 'architecture' (ex: arm v8) and for their 'implementation' (ex: ARM11), and maybe it all makes sense if you have drunk the ARM cool-aid and have joined the ARM cult, but to sane people and outsiders, it is just a f*cking mess."*

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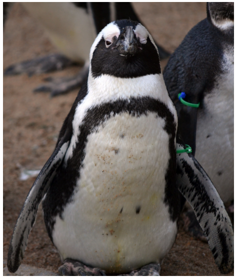

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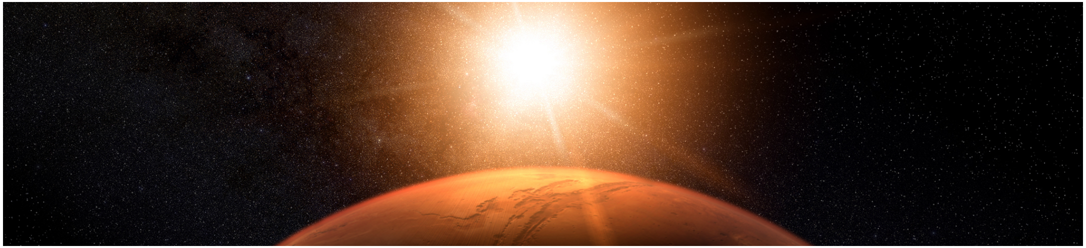
So let's drink the 'ARM cool-aid' and figure out what's going on…

Documentation: off to a good start



Everything you need to know is described in a handy book!

- Hilariously called the 'Arm ARM' (miraculously, you can search for this)
- Almost 8000 pages long
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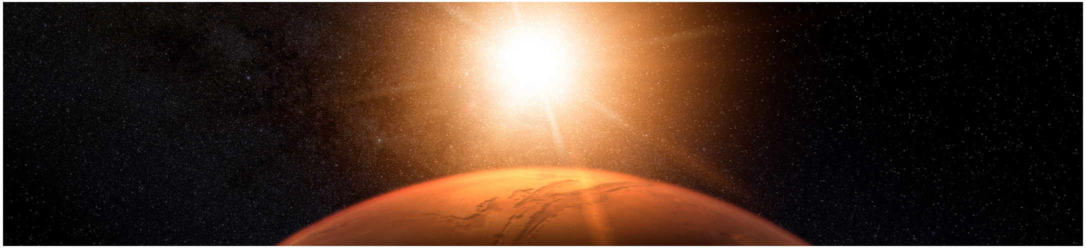

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- Did you know? If you printed a copy for every shipped CPU, it would reach Mars and back 500x!

The Arm ARM: Maybe not so handy after all?

“Any interrupt that is pending before a Context synchronization event in the following list, is taken before the first instruction after the context synchronizing event, provided that the pending interrupt is not masked:

- *Execution of an ISB instruction.*
- *Exception entry, if ARMv8.5-CSEH is not implemented, or if ARMv8.5-CSEH is implemented and the appropriate SCTLR_ELx.EIS bit is set.*
- *Exception return, if ARMv8.5-CSEH is not implemented or if ARMv8.5-CSEH is implemented and the appropriate SCTLR_ELx.EOS bit is set.*
- *Exit from Debug state.”*

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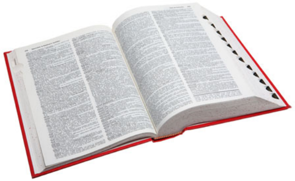
This is not the 'cool-aid' you are looking for.

Hurdle 1: Arm is mostly inaccessible to developers on the outside.

Important terminology



- Architecture vs micro-architecture
- Core license vs architecture license
- Diversity vs fragmentation
- CPU vs SoC
- ISA vs system architecture

Understanding these differences is crucial to picking apart and understanding the Arm ecosystem.

Architecture vs Micro-architecture

Architecture is the contract between hardware and software. It describes the portable guarantees provided by the hardware, without dictating how they are implemented, and is typically specified in English. Arm has three architecture *profiles*: A, R and M (more hilarity). Approx. 5yr lag.

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Hurdle 2: This distinction is far less significant on other architectures such as x86.

Hysterical raisins

<=ARMv4	*When dinosaurs roamed the Earth*
ARMv5	2000, Baseline, Xscale
ARMv6	2002, SMP (sort of), ARM11
ARMv7-A	2005, Virtualisation, VMSA architecture, Cortex-A8
Armv8-A	2011, 64-bit ISA (AArch64), Cortex-A53

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Armv8.2-A	2015, RAS extensions, Cortex-A77
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Hurdle 3: Many features optional! Discoverable at runtime using ID registers.

Licensing

Why is the product naming so inconsistent? *Partly* due to the licensing model:

Core license to include a specific Arm CPU design in your SoC. Minor modification may be permitted.

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Hurdle 4: Important that Arm doesn't produce production silicon as an SoC

The Arm ecosystem

Playing ‘Switzerland’

Arm’s influence is in the power of the partnership and underlying platform; on its own, it’s relatively tiny in revenue terms:

Qualcomm	22B USD (2018)
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Hurdle 5: Limited ability to mandate standards compliance or move goalposts

Diversity vs Fragmentation

‘Pick ‘n’ mix’ architecture reigned in slightly by desire for software re-use:

PSCI	to bring CPUs up and down
SBSA	certification for server system designs
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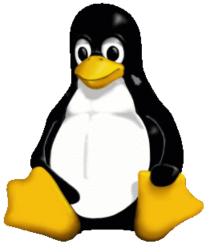
Hurdle 6: Still a tendancy towards fragmentation between SoCs

`https://www.mono-project.com/news/2016/09/12/arm64-icache/`

How does Linux cope?

The `arm64` Linux kernel is written to the *architecture* and aims to abstract away the underlying bag of bits baked into silicon:

- Single `defconfig` binary image for all AArch64 CPUs
- Heavy use of ‘alternative’ instruction patching
- uarch-specific features not worth the effort…
- …apart from errata workarounds and side-channels
- Heterogeneous systems are a headache
- Exposed to userspace via `proc`, `sys`, `ELF HWCAP` and `MRS` instructions



Details in `Documentation/arm64/cpu-feature-registers.rst`

Email the list if you need more: `linux-arm-kernel@lists.infradead.org`

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Fire up the simulation

Where do I start? / What’s in the box?

1. Ignore all the marketing junk
2. Identify the SoC
3. Identify the CPU(s) – Arm derived?
4. Identify architecture version
5. Identify features
6. `https://wikichip.org`

Some example devices

Example 1: Libre Computer ‘La Frite’

They say…

AML-S805X-AC is the perfect development platform for projects that require highly performant ARM Cortex-A class CPUs, small compact form factor, secure and non-secure 1080P media delivery and playback, high reliability, and low power.

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- Soc is Amlogic S805x
- 4x ARM Cortex-A53 @ 1.2GHz
- Cortex-A53 is a 64-bit core implementing ARMv8.0
- Usually the ‘Little’ in early ‘big.Little’ designs

ARM says…

The most widely-used processor with balanced performance and efficiency

Example 2: Samsung Galaxy S9

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10nm 64-bit Octa-Core Processor 2.8GHz + 1.7GHz (Maximum Clock Speed, Performance Core + Efficiency Core)

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The Cortex-A55 implements more instructions than the Mongoose 3!

`https://medium.com/@jadr2ddude/a-big-little-problem-a-tale-of-big-little-gone-wrong-e7778ce744bb`

Example 3: Motorola moto z4

They say…

Feel the speed of a Qualcomm® Snapdragon™ 675 processor that's 57% faster than moto z3 play. It's a phone built to keep up with you.

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- Wikichip to the rescue!
- Kryo 460 Silver => Cortex-A55
- Kryo 460 Gold => Cortex-A76
- Both implement ARMv8.2

'The two big disclosed changes are an increase of the core's reorder buffer from 128 entries to a higher, unspecified amount, as well as tuning the prefetchers to better work with floating point workloads.' https://www.anandtech.com/show/14072/the-samsung-galaxy-s10plus-review/3

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Questions?

Please contact `support@arm.com`!

Image references

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